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PATENT; Atty Docket No. BBE1199-CIP
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TRANSMITTAL

Transmitted herewith for filing is the PATENT APPLICATION of Inventor: Paul R. Gagon

For: AN AUDIO BOOST CIRCUIT

[X] 4 sheets of drawing. (4 Figures)
[X] A Power Of Attorney.
[X] A Declaration Of Invention.
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BASIC FEE			$380	380.
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Respectfully submitted, Signature James F. Kirk 11/22/99

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In re: Application of: Paul R. Gagon
| Examiner:

For: **AN AUDIO BOOST CIRCUIT**
Attorney Docket No. BBE1199-CIP
Serial No.: ____________________ | Group Art Unit:

Filed: Herewith

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EXPRESS MAIL CERTIFICATE (37CFR 1.10)

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I hereby certify that the following attached paper and fee:

Application specification including 17 claims and
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Typed Name of Person Mailing: James F. Kirk

Applicant: Atty. Dkt. No.

Application Serial No. :

Filed:

For:

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) AND 1.27 (c)) — SMALL BUSINESS CONCERN

I hereby declare that I am

( ) the owner of the small business concern identified below:

(X) an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN: BBE Sound, Inc.

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18 and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, titled: AN AUDIO BOOST CIRCUIT ________________ by inventor(s) PAUL R. GAGON.

described in

(X) the specification filed herewith

( ) application serial no.________________, filed ________________

( ) patent no __________, issued ________________

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

* NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities: (37 CFR 1.27)

NAME: ________________________

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( ) INDIVIDUAL ( ) SMALL BUSINESS CONCERN ( ) NONPROFIT CORPORATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate: (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

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TITLE OF PERSON OTHER THAN OWNER: Chairman / CEO

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DATE: November 22, 1999

015.404190

An Audio Boost Circuit

This patent application is a continuation-in-part application of parent application having serial number 09/439,119 filed 11/12/99.for an Audio Boost Circuit having a common inventor and assignee.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to the field of electronics amplifiers and more particularly to the field of signal conditioning circuits for signal boosting in within a predetermined bandwidth so as to compensate for reduced speaker performance resulting from reduced woofer size.

2. Description of Related Art:

U.S. Patent 5,736,897 for a Low Input Signal Bandwidth Compressor & Amplifier Control Circuit with a State-variable Pre-Amplifier issued on April 7, 1998 to Paul Gagon who assigned the invention to BBE Sound of Huntington Beach, California. The contents of U.S. Patent 5,736,897 are incorporated by reference herein in its entirety. The inventor and assignee are common with those for the present invention. The `897' patent shows the use of a state-variable filter. The `897' reference does not show or teach the use of an Infinite Gain Multiple Feedback Band-Pass Filter in combination with a State-Variable Band-Pass Filter acting as a pre-amplifier.

SUMMARY OF INVENTION

In a first embodiment, the invention audio boost circuit has input buffer responsive to a program input signal having high, low and mid-range frequency signal components for providing a buffered program signal. The buffered program signal is fed to an all pass phase inverter having an input coupled to receive the buffered program signal and an output providing an inverted buffered program signal, The buffered program signal is also fed to a band pass filter having a predetermined Q, responsive to the buffered program signal for providing an inverted band pass boosted program signal. A summing amplifier adds the inverted buffered program signal to the inverted band pass boosted program signal to provide a composite program signal signal as an output signal to a power amplifier and speaker combination. In a more particular embodiment, the band pass filter has a peak gain at a center frequency, and, a frequency adjustment means is provided for adjusting the frequency at which the peak gain occurs. In a yet more particular embodiment, the band pass filter has a first second and third resistor and a first and second capacitor, and the band pass filter's first, second and third resistor values and the values of the first and second capacitors are selected to obtain a Q in the range of from 3 to 6, and a frequency adjustment resistor in series with the second resistor is adjusted to position the peak gain at a frequency in the range of 50 to 100 cycles/sec.

A second alternative embodiment of the invention audio boost circuit comprises an input buffer responsive to a program input signal having high, low and mid-range frequency signal components for providing a buffered program signal, the

input buffer comprises: a state-variable filter for processing the input program signal into high, low and mid-range frequency compensated signal components. The state-variable filter comprises: a first amplifier stage responsive to the program signal that provides a high frequency compensated signal; a second amplifier stage responsive to an output of the first amplifier stage that provides a mid-range compensated signal; and, a third amplifier stage responsive to an output of the second amplifier stage that provides a low range compensated signal.

The input buffer further comprises: a state-variable summing amplifier for adding the high frequency compensated signal, the low frequency compensated signal and the mid-range compensated signal and an adjusting means for adjusting the gain between the high frequency compensated signal and the mid-range compensated signal; and the low frequency compensated signal to provide the buffered program signal.

The input buffer is followed by an all pass phase inverter having an input coupled to receive the buffered program signal and an output that provides an inverted buffered program signal, A band pass filter with a predetermined Q, is coupled to the buffered program signal to provide an inverted band pass boosted program signal, A summing amplifier adds the inverted buffered program signal to the inverted band pass boosted program signal to provide a composite program signal. A power amplifier and speaker respond to the composite program signal to producing an audible sound in response to the composite program signal.

In a more particular second embodiment, of the state-

variable filter, the mid-range signal components are inverted in phase with respect to the high and low frequency signal components and the state-variable filter further comprises: a first amplifier stage having an inverting and non-inverting input. The program signal is coupled to the inverting input; and a resistor divider network is coupled to the mid-range compensated signal. The resistor divider network has an output that provides a portion of the mid-range compensated signal to the first amplifier non-inverting input.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1. is a block diagram of the audio boost circuit;

Figure 2 is a schematic of the block diagram of Figure 1 showing a first embodiment of an input buffer, the all pass phase inverter, the constant Q band pass filter and the summing amplifier.

Figure 3 is an expanded block diagram of Figure 1 showing a second embodiment of the input buffer;

Figure 4 is a schematic of the expanded block diagram of the second embodiment of the input buffer.

PREFERRED EMBODIMENT

Figure 1. is a block diagram of the audio boost circuit 10 showing an input buffer 12 having an input 14 and an output at terminal 16. An all pass phase inverter 18 has its input connected to terminal 16 and its output is connected to terminal 20. A constant Q band pass filter 22 has its input connected to terminal 16 and its output connected to terminal 24. Summing amplifier 26 has a first input connected to terminal 20, a second input connected to terminal 24 and an output connected to terminal 28. Block 30 represents a power amplifier having an input connected to the transfer contact 32 of switch 34. The power amplifier output 36 is shown connected to a speaker 38.

The input buffer 12 is coupled to receive a program input signal at input terminal 14. The program input signal is typically received from a tape player or a CD reader. Such signals typically contain audio information such as recorded music and have amplitudes in the range of 150 mV RMS and have high, low and mid-range frequency audio signal components for providing a buffered program signal at terminal 16.

The all pass phase inverter 18 has an input coupled to receive the buffered program signal at terminal 16 and an output providing an inverted buffered program signal to terminal 20.

The band pass filter 22 is designed to have a predetermined Q with a center frequency that is empirically selected to optimize the performance of the power amplifier 30 and speaker 38. The band pass filter 22 is connected to receive

the buffered program signal from terminal 16 and amplify and phase invert a narrow range of low frequency of the buffered program signal to provide an inverted band pass boosted program signal to terminal 24,

Summing amplifier 26 adds the inverted buffered program signal received at its first input from terminal 20 to the inverted band pass boosted program signal received at its second input from terminal 24 and outputs the sum of the signals as a composite program signal signal at terminal 28.

Figure 2 is a schematic of a first embodiment of the audio boost circuit. The component values show were used in a circuit that was built and tested. Phantom block 12 shows the input buffer comprising a simple unity gain non-inverting amplifier. An inverting unity gain amplifier would work equally as well. The amplifier shown in 1/4 of a TL072. The 10 uF capacitor is a dc blocking capacitor. The 100 pF capacitor is for high frequency noise suppression. A second embodiment of the input buffer using a state-variable filter is discussed later in connection with Figures 3 and 4.

The all pass phase inverter within phantom block 18 is an inverting unity gain amplifier. The 100 pF capacitor is used to enhance the stability of the operational amplifier. The band pass filter within phantom block 22 is designed to have a predetermined Q in the range of from 3 to six. The Q selected and the center frequency selected are empirically determined with the power amplifier and speaker combination for best results. The band pass filter has resistors first second and third resistors 40, 42 and 44 respectively, each resistor having a first and second terminal, The filter also

has a first and second capacitor, 46 and 48 respectively each capacitor having a first and second terminal. Operational amplifier 50 has an inverting input, a non-inverting input and an output connected to terminal 24.

The first resistor 40 first terminal is coupled to terminal 16 to receive the buffered program signal. The first resistor second terminal is coupled or connected to node 52. The second resistor 42 first terminal and the first terminal of the first and second capacitors 46, 48 are also connected to node 52.

The second resistor 42 second terminal is connected to a reference potential such as ground. In the embodiment of Figure 2, adjustable resistor 54 is connected in parallel with resistor 56 and the pair are in series with resistor 42 to form a frequency adjustment means for adjusting the frequency at which the peak gain of the band pass filter 22 occurs. The adjustment means could be a single equivalent value resistor selected to replace the second resistor 42 in series with the parallel combination of the adjustable resistor 54 and resistor 56.

The first capacitor 46 second terminal is connected to the operational amplifier's inverting input and to the third resistor's 44 first terminal. The second capacitor's 48 second terminal is connected to the operational amplifier's output terminal and to the third resistor's 44 second terminal.

The band pass filter of phantom block 22 is referred to as an infinite gain multiple feedback band pass filter. The design of an infinite gain multiple feedback band pass

filter such as shown in phantom block 22 in Figure 2 is taught with examples given in the text "The Active Filter Handbook" by Frank P. Tedeschi, pg 160 - 168, Tab Books Inc of Blue Ridge Summit, Pa., 17214.

An alternative discussion with design examples is found in the "Handbook Of Operational Amplifiers Active RC Networks" 1966, at pages 32 - 34 and 78 - 79, published by the BURR-BROWN RESEARCH, CORPORATION, INTERNATIONAL AIRPORT INDUSTRIAL PARK, TUCSON, ARIZONA 85706.

However, the topology for a set of design requirements is not unique nor are the values for a given topology. The following example and equations show how the component values are determined for an circuit in which the Q, center frequency f and the peak gain Ao are given. In general, the Q of a band-pass filter is defined as the bandwidth divided by the center frequency. Assume that the center frequency required is 78.8 Hz. Assume that the Q required is 5.4 and the peak gain Ao required is 1.03. The first and second capacitors have the same value which is defined as c. A convenient value of 0.39 uF is selected for a first try. Using the design procedure found in the "Handbook Of Operational Amplifiers Active RC Networks" mentioned above:

$c \equiv 0.39 \cdot 10^{-6}$ $\quad Q \equiv 5.4$ $\quad f \equiv 78.7$ $\quad Ao \equiv 1.03$

$a := \dfrac{1}{Q}$ $\quad k \equiv 2 \cdot \pi \cdot f \cdot c$ $\quad \pi \equiv 3.14159$

$a = 0.185$ $\quad k = 1.928 \cdot 10^{-4}$ $\quad H := \dfrac{Ao}{Q}$

$$R1 := \frac{1}{H \cdot k} \qquad R2 := \frac{1}{(2 \cdot Q - H) \cdot k} \qquad R3 := 2 \cdot \frac{Q}{k}$$

$$R1 = 2.719 \cdot 10^{4} \qquad R2 = 488.76 \qquad R3 = 5.6 \cdot 10^{4}$$

With a Q of 3 specified, the following values of resistors were calculated using the same value of capacitors:

$$R1 = 1.51 \cdot 10^{4} \qquad R2 = 916.686 \qquad R3 = 3.111 \cdot 10^{4}$$

The values of R1, R2 and R3 corresponds to the values of the first, second and third resistors in the previous example. It can be seen that the values of resistors are obtainable for the range of Q of 3 to 6 that is desired. The frequency adjustment resistor 54 and the values of resistors 42 and 56 which combine to form R2 in the calculations above are calculated or determined empirically to position the peak gain at a frequency in the range of 50 to 100 herts.

The summing amplifier within phantom block 26 represents a means for adding the inverted buffered program signal to the inverted band pass boosted program signal and for providing a composite program signal. Resistor 58 has a first and second terminal. The first terminal of resistor 58 is connected to terminal 20 to receive the inverted buffered program signal. The second terminal of resistor 58 is connected to the inverting input of operational amplifier

and to the first terminal of the feed-back resistor 62. The second terminal of the feedback resistor 62 is connected to the output of the summing amplifier terminal 28.

Resistor 64 and 66 in series have a first and second terminal. The first terminal of the series combination is connected to terminal 24 to receive the inverted buffered program signal. The second terminal of the series combination is also connected to the inverting input of operational amplifier and to the first terminal of the feed-back resistor 62. The first terminal of the series combination is connected terminal 24 to receive the inverted band pass boosted program signal from the band pass filter.

Adjustable resistor 66 in series with resistor 64 represent a boost adjusting resistor in series with the second input to the summing amplifier for adjusting the relative gain of the inverted buffered program signal with respect to the inverted band pass boosted program signal.

Figure 3 is shows the block diagram of a second alternative embodiment of the input buffer 12 using a state-variable filter 72 responsive to the program input signal at terminal 14 having high, low and mid-range frequency signal components. This second embodiment of the input buffer 12 has a state-variable filter 72 and a state-variable summing amplifier 74 for adding the high, low and mid-range frequency signal components to provide the buffered program signal.

The state-variable filter has a first amplifier stage 90

responsive to the program signal for providing a high frequency compensated signal; a second amplifier stage 98 responsive to an output of the first amplifier stage for providing a mid-range compensated signal; and a third amplifier stage 104 responsive to the mid range compensated signal for providing a low range compensated signal.

In Figure 4, the input buffer 12 has gain control circuitry within the state-variable summing amplifier 74, such as adjustable resistors 114 and 116, for balancing and summing the high and mid-range signals.
The state-variable filter within phantom box 72 is coupled or connected to the program input signal at terminal 14 and processes the program input signal into high, low and mid-range frequency signal components. The state-variable summing circuit 74 adds the high frequency compensated signal, the low frequency compensated signal and the mid-range compensated signal to provide the buffered program signal at terminal 16. The input buffer also provides an adjusting means within the state-variable summing amplifier 74 for adjusting the gain between the high frequency compensated signal and the mid-range signal.

The three band-pass signals comprise a low band-pass signal Vlp (a low-range compensated signal) on signal line 76, a mid-range bandpass signal Vmp (a mid-range compensated signal) on signal line 78 and a high range bandpass signal, Vhp (a high frequency compensated signal) on signal line 80 to respective inputs of a state-variable summing amplifier 74. The mid-range signal components produced by the state-variable filter 72 are inverted in phase with respect to the phase of the high and low frequency signal components produced by the state-variable filter 72.

Figure 4 shows that the state-variable summing amplifier 74 uses operational amplifier 82 and sums the respective Vlp, Vmp and Vhp signals at the low pass input 84, the mid-range input 86 and the high pass input 88, and provides the buffered program signal at output terminal 16 to the all pass phase inverter 18 and to the band pass filter 22 as shown in Figure 1 ,or via switch 34, directly to power amplifier 30 to drive speaker 38.

As explained in U.S. Patent 5,736,897 for a Low Input Signal Bandwidth Compressor & Amplifier Control Circuit with a State-variable Pre-Amplifier issued on April 7, 1998, the combination of the state-variable filter 72 and the state-variable summing amplifier 74 form a functional and lower cost equivalent of the alternative embodiment three channel pre-amplifier shown in Figures 1 and 2 in the `897' patent.

Referring again to Figures 3 and 4, phantom block 90 represents an input summing and damping amplifier circuit. The program input signal at terminal 12 and the low bandpass signal Vlp on signal line 76 are fed to the inverting input of amplifier 92. A portion of the mid-range band-pass signal Vmp is fed to the non-inverting input of amplifier 92 for damping via the damping input 94. The resulting output of amplifier 92 was the high frequency signal component Vhp at amplifier output 96 which was connected to signal line 80,

The high range band-pass signal Vhp is then connected to the negative input of a first integrator shown within phantom block 98, for inversion and integration and to the state-variable summing amplifier 74 high pass input 100 on signal line 80.

The first integrator 98 integrates the Vhp signal to provide the mid-range band-pass signal Vmp at first integrator output 102. The mid-range bandpass signal Vmp is fed to the damping input 94 of the input summing and damping amplifier circuit 90 and to the state-variable summing amplifier 92 mid-range band-pass input 86 on signal line 78.

Phantom block 104 represents a second integrator that responds to the mid-range bandpass signal Vmp on signal line 78 and provides a low bandpass signal Vlp at the second integrator output terminal 106 to the state-variable summing amplifier 74 low band-pass signal input 84 via signal line 76. The low bandpass signal Vlp is also fed to a second input 108 of the input summing and damping amplifier circuit 90.

The damping circuit of the input summing and damping amplifier circuit 90 comprises an input resistor 110 that has a first terminal connected to receive the mid-range bandpass signal at damping input 94. The second terminal of resistor 110 is coupled to the first terminal of resistor 112 and to the non-inverting input of operational amplifier 92. The second terminal of resistor 112 is coupled to a reference potential such as ground. The ratio of resistors 110 and 112 establish the "Q" of the state-variable filter. The higher the gain, of the ratio of the resistors 110 and 112, the higher the Q. The Q of the state-variable filter of Figures 3 and 4 is typically in the range of 0.5 to 2 for audio applications. The Q of the circuit of Figure 4 is approximately 0.67.

One of the objectives of the state-variable filter 72 is to set phase shift and gains up such that the mid-range band-

pass frequency signals are about 180 degrees out of phase with the signal components in the lower frequency band and in the higher frequency band. The ratio of the damping resistors, the gains and break frequencies of the amplifiers and integrator are set for a desired Q and bandpass.

The state variable summing amplifier 74 has a low frequency band-pass gain adjustment pot 114, and a high range band-pass frequency gain adjustment pot 116 that permit the user to make a final adjustment for a particular circuit and component configuration. The adjustable inputs to the state variable summing amplifier 74 permit the user to obtain additional gain for the Vhp and Vlp signal.

The state variable input buffer circuit of Figures 3 and 4 can be adjusted to obtain a total of 360 degrees of phase shift of the high frequency signal components of the input program signal with respect to the low frequency signal components of the input program signal, in frequency space over the range of 0 - 20,000 Hz. The high frequency components gain 360 degrees with respect to the lows.

The state variable pre-amplifier also provides a time delay that is adjusted to obtain about 2.5 ms time delay at 20 Hz. The 20 Hz components are physically delayed in real time by up to 2.5 ms with respect to the High Frequency components. The design objectives for audio applications are taught in U.S. Patent 4,638,258 issued on January 20, 1987 for a Reference Load Amplifier Correction System, to Robert C. Crooks. The contents of U.S. Patent 4,638,258 are incorporated herein by reference in its entirety.

Referring again to Figure 4, a reactance chart check

will show that the break frequency for the mid-range bandpass amplifier 98 to be about 2.24 KHz. The break frequency for the low range bandpass amplifier 104 is about decade lower at 224 Hz at three dB per octave. The Q of the circuit of Figure 4 is approximated by the following equation:

$$Q = (R1 + R2)/3R2 = 0.67$$

where R1 is resistor 110 and R2 is resistor 112.

Viewing the circuit heuristically, the higher reactance of the smaller cap for mid-range bandpass amplifier 98 clearly sets the gain of the amplifier to higher values at lower frequencies than that of the low range band-pass amplifier 104. It can also be seen that the mid-range band-pass amplifier is a single pole filter. The feed back signal Vmp to the damping resistors results in a controlled Q in the mid-range frequencies band.

In general, the Q of a band-pass filter is defined as the bandwidth divided by the center frequency. The design of the state variable filter of Figure 4 is taught in the text "The Active Filter Handbook" by Frank P. Tedeschi, pg 178 - 182, Tab Books Inc of Blue Ridge Summit, Pa., 17214; however, this reference does not show the outputs being summed to form the desired unbalanced output that meets the desired requirement for audio applications.

The object of the design of Figure 4 is to have a first break frequency at approximately 240 Hz and a second at 2.24 KHz, about a decade away from the first break. The low break f_c is established by the equation:

$$fc = 1/2\pi RC2$$

where R and C are the value of resistor 116 and capacitor 118. The high frequency break is set by the

$$fc = 1/2\pi RC1$$

where the value of R and $_{C1}$ are those of resistor 120 and capacitor 122.

Once the Q is selected, the ratio of R1 to R2 can be calculated from the equation. In the case of Figure 4, a Q of 0.67 was selected by knowing what the desired gain bandwidth response curve would be from the above referenced U.S. Patent 4,638,258. The circuit was modeled using a computer aided analysis program such as SPICE. The break frequencies were estimated from the information in the referenced U.S. Patent 4,638,258. Initial component values were selected based on available components. A reactance chart can be used for a quick approximation of the required remaining value once one of the values are known. The circuit shown had an initial goal of a design a center frequency at 700 Hz. At the center frequency, the gain of the circuit is about -1 dB or less than 1. The two adjustment pots, 116 and 114 permit an adjustment of the gain of the Vlp and the Vhp by about 15 dB with the values shown.

The Q was then adjusted using the pots 114 and 116 to provide the best match to the curves in the earlier patent to Crook. The Q and the break points were selected to match the response characteristic of the resulting circuit to the curves in the earlier patent to yield the same phase shifts, time delays and frequency response. The resistors 114 and

116 are set for a gain of nine but a slightly higher gain of 12 would be preferred.

The outputs Vhp, Vmp and Vlp of the state variable filer represent three independent state variables. Summing the three unbalanced outputs to obtain a buffered program signal is believed to be a novel step when combined with processing by the all pass inverter 18 in combination with the band pass filter 22 and with the resulting signals being summed by summing amplifier 26.

The procedure for adjusting the band-pass and gain as proposed in the above referenced text "The Active Filter Handbook" by Frank P. Tedeschi, at pages 178 - 182" is to set the value of C1 and C2 to be equal and to adjust the ratio of R1 and R2 and to obtain the desired Q. In the circuit of Figure 4, the state-variable summing amplifier 74 gain controls for the Vhp and Vlp signals provide for independent control of the gain and band-pass.

The above-described embodiments are furnished as illustrative of the principles of the invention, and are not intended to define the only embodiment possible in accordance with our teaching. Rather, the invention is to be considered as encompassing not only the specific embodiments shown, but also any others falling within the scope of the following claims.

I Claim:

1. An audio boost circuit comprising:

an input buffer responsive to a program input signal having high, low and mid-range frequency signal components for providing a buffered program signal,

an all pass phase inverter having an input coupled to receive the buffered program signal and an output providing an inverted buffered program signal,

a band pass filter having a predetermined Q, responsive to the buffered program signal for providing an inverted band pass boosted program signal,

a summing amplifier for adding the inverted buffered program signal to the inverted band pass boosted program signal and for providing a composite program signal signal.

2. The audio boost circuit of claim 1 wherein the band pass filter having a predetermined Q has a peak gain at a center frequency, and,

frequency adjustment means for adjusting the frequency at which the peak gain occurs.

3. The audio boost circuit of claim 2 wherein the band pass filter having a predetermined Q further comprises:

a first, second and third resistor, each having a first and second terminal,

a first and second capacitor, each capacitor having a first and second terminal, and

an operational amplifier having an inverting input, a non-inverting input and an output,

the first resistor first terminal being coupled to receive the buffered program signal, the first resistor second terminal being coupled to the second resistor first

terminal and to the first terminal of the first and second capacitors, the second resistor's second terminal being coupled to a reference potential, the first capacitor second terminal being connected to the operational amplifier's inverting input and to the third resistors first terminal, the second capacitor's second terminal being connected to the operational amplifier's output terminal and to the third resistor's second terminal.

4. The audio boost circuit of claim 3 wherein the band pass filter frequency adjustment means for adjusting the frequency at which the peak gain occurs comprises:

a frequency adjustment resistor interposed in series with the second resistor and the reference potential.

5. The audio boost circuit of claim 4 wherein the band pass filter's first, second and third resistor values and the values of the first and second capacitors are selected to obtain a Q in the range of from 3 to 6, and

the frequency adjustment resistor is adjusted to position the peak gain at a frequency in the range of 50 to 100 herts.

6. The audio boost circuit of claim 1 wherein the summing amplifier for adding the inverted buffered program signal to the inverted band pass boosted program signal and for providing a composite program signal further comprises:

a first input coupled to receive the inverted buffered program signal and a second input coupled to receive the inverted band pass boosted program signal, and adjustment means for adjusting the relative gain of the inverted buffered program signal with respect to the inverted band pass boosted program signal.

7. The audio boost circuit of claim 6 wherein the adjustment means for adjusting the relative gain of the inverted buffered program signal with respect to the inverted band pass boosted program signal further comprises a boost adjusting resistor in series with the second input to the summing amplifier.

8. The audio boost circuit of claim 1 wherein the input buffer for providing a buffered program signal further comprises:

an input buffer connected to receive the program input signal and for processing the input program signal to provide high, low and mid-range frequency signal components, the input buffer having gain control circuitry for balancing and summing the high and mid-range signals.

9. The audio boost circuit of claim 8 wherein the input buffer further comprises:

a state-variable filter responsive to the program input signal for producing high, low and mid-range frequency signal components; and

a state-variable summing amplifier for adding the high, low and mid-range frequency signal components to provide the buffered program signal.

10. The audio boost circuit of claim 9 wherein the mid-range signal components produced by the state-variable filter are inverted in phase with respect to the phase of the high and low frequency signal components produced by the state-variable filter .

11. An audio boost circuit comprising:

an input buffer coupled to be responsive to a program

input signal having high, low and mid-range frequency signal components, the input buffer having a state-variable filter for processing the program input signal into high, low and mid-range frequency signal components, and a state-variable summing amplifier for balancing and summing the low, high and mid-range signal components and for providing the buffered program signal,

an all pass phase inverter having an input coupled to receive the buffered program signal and an output providing an inverted buffered program signal,

a band pass filter having a predetermined Q, responsive to the buffered program signal for providing an inverted band pass boosted program signal,

a summing amplifier for adding the inverted buffered program signal to the inverted band pass boosted program signal and for providing a composite output signal.

12. The audio boost circuit of claim 11 wherein the input buffer's state-variable filter for providing a compensated signal further comprises:

a first amplifier stage responsive to the program signal for providing a high frequency compensated signal;

a second amplifier stage responsive to an output of the first amplifier stage for providing a mid-range compensated signal;

a third amplifier stage responsive to the mid range compensated signal for providing a low range compensated signal; and

a state-variable summing circuit for adding the high frequency compensated signal, the low frequency compensated signal and the mid-range compensated signal to provide the buffered program signal.

13. The audio boost circuit of claim 12 wherein the mid-range compensated signal is out of phase with the high range and low range compensated signals.

14. The audio boost circuit of claim 13 wherein the input buffer's state-variable filter for providing a buffered program signal further comprises:

an adjusting means for adjusting the gain between the high frequency compensated signal and the mid-range signal.

15. An audio boost circuit comprising:

an input buffer responsive to a program input signal having high, low and mid-range frequency signal components for providing a buffered program signal, the input buffer comprising:

a state-variable filter for processing the input program signal into high, low and mid-range frequency compensated signal components, the state-variable filter comprising:

a first amplifier stage responsive to the program signal for providing a high frequency compensated signal;

a second amplifier stage responsive to an output of the first amplifier stage for providing a mid-range compensated signal; and,

a third amplifier stage responsive to an output of the second amplifier stage for providing a low range compensated signal;

the input buffer further comprising:

a state-variable summing circuit for adding the high frequency compensated signal, the low frequency compensated signal and the mid-range compensated signal and an adjusting means for adjusting the gain between the high frequency compensated signal and the mid-range compensated signal; and

the low frequency compensated signal to provide the buffered program signal;

an all pass phase inverter having an input coupled to receive the buffered program signal and an output providing an inverted buffered program signal,

a band pass filter having a predetermined Q, responsive to the buffered program signal for providing an inverted band pass boosted program signal,

a summing amplifier for adding the inverted buffered program signal to the inverted band pass boosted program signal and for providing a composite program signal, and

a power amplifier and speaker means responsive to the composite program signal for producing an audible sound in response to the composite program signal.

16. The audio boost circuit of claim 15 wherein the mid-range signal components are inverted in phase with respect to the high and low frequency signal components.

17. The audio boost circuit of claim 15 wherein the input buffer's state-variable filter further comprises:

a first amplifier stage having an inverting and non-inverting input; the program signal being coupled to the inverting input; and

a resistor divider network responsive to the mid-range compensated signal, the resistor divider network having an output for providing a portion of the mid-range compensated signal to the first amplifier non-inverting input.

ABSTRACT

An audio boost circuit having an input buffer responsive to a program input signal for providing a buffered program signal, An all pass phase inverter having an input coupled to receive the buffered program signal and an output providing an inverted buffered program signal. A band pass filter having a predetermined Q, responsive to the buffered program signal for providing an inverted band pass boosted program signal. A summing amplifier for adding the inverted buffered program signal to the inverted band pass boosted program signal and for providing a composite program signal signal. A frequency adjustment means for adjusting the frequency at which the peak gain occurs. The input buffer is a state-variable input filter that processes the program input signal into high, low and mid-range frequency signal components. The input buffer has gain control circuitry for balancing and summing the high and mid-range signal components. A state-variable band-pass active filter processes the program input signal to produce the high, low and mid-range frequency signal components. A summing circuit adds the high, low and mid-range frequency signal components to provide the buffered program signal.

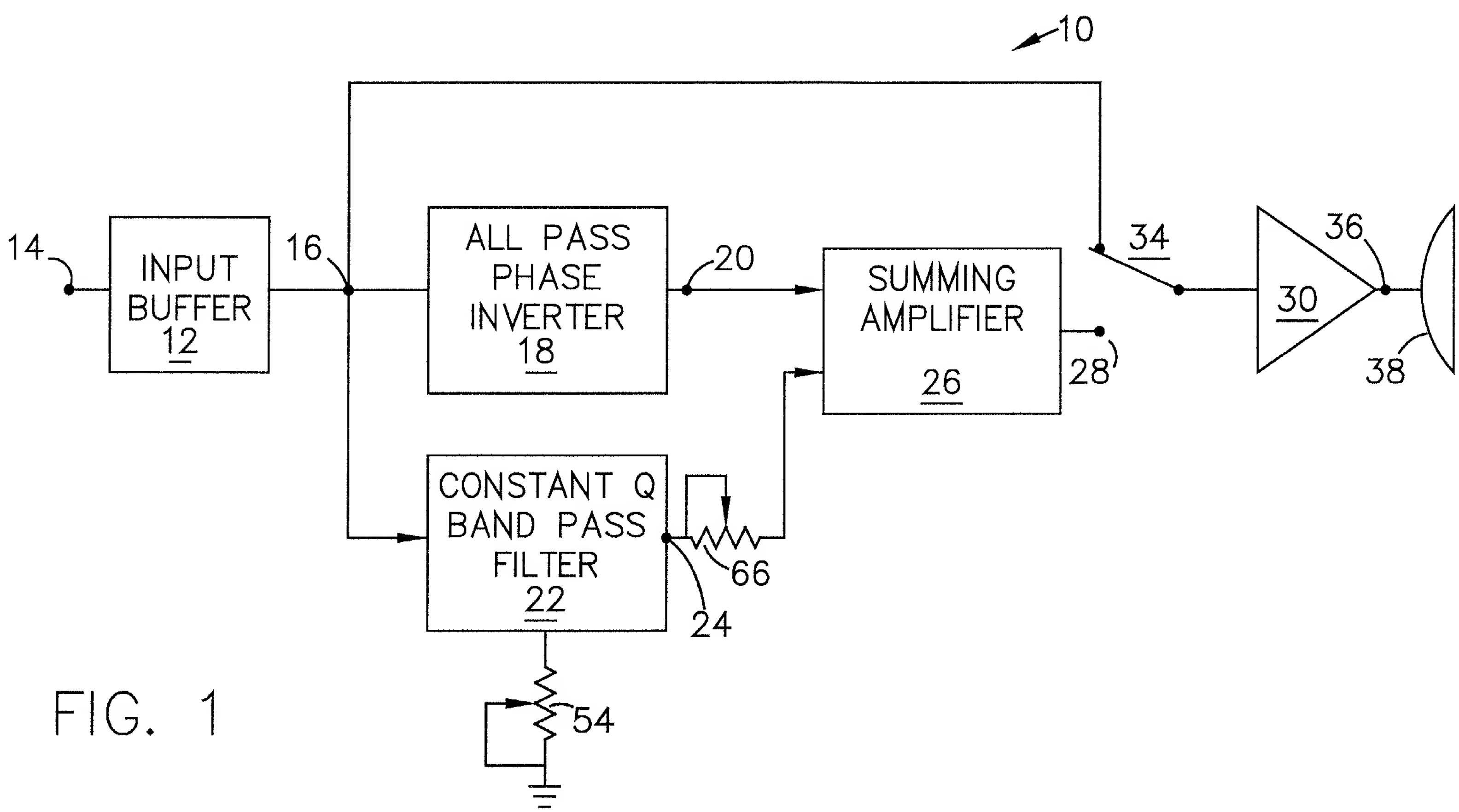
10
14
INPUT BUFFER 12
16
ALL PASS PHASE INVERTER 18
20
SUMMING AMPLIFIER 26
28
34
30
36
38
CONSTANT Q BAND PASS FILTER 22
24
66
54

FIG. 1

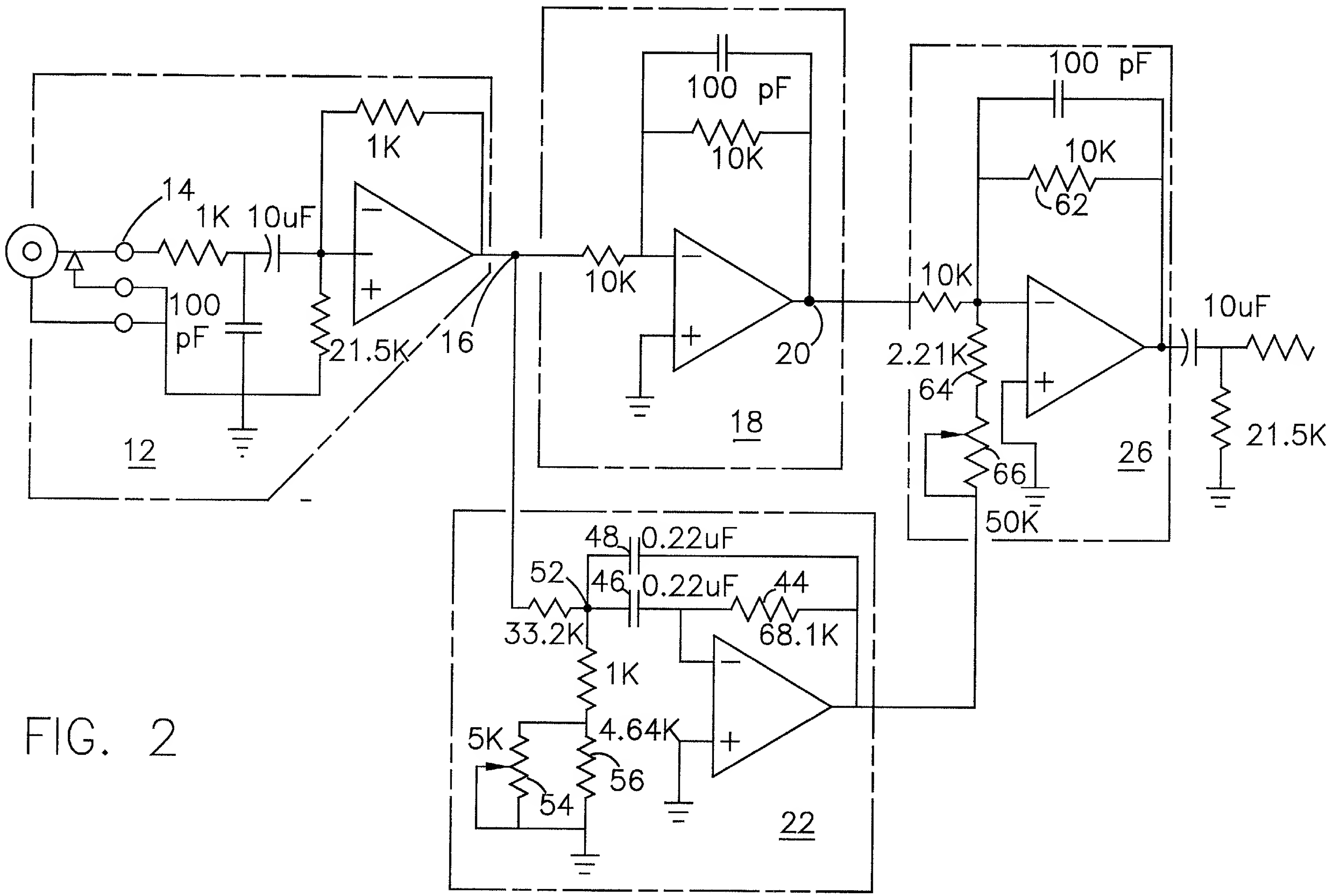

FIG. 2

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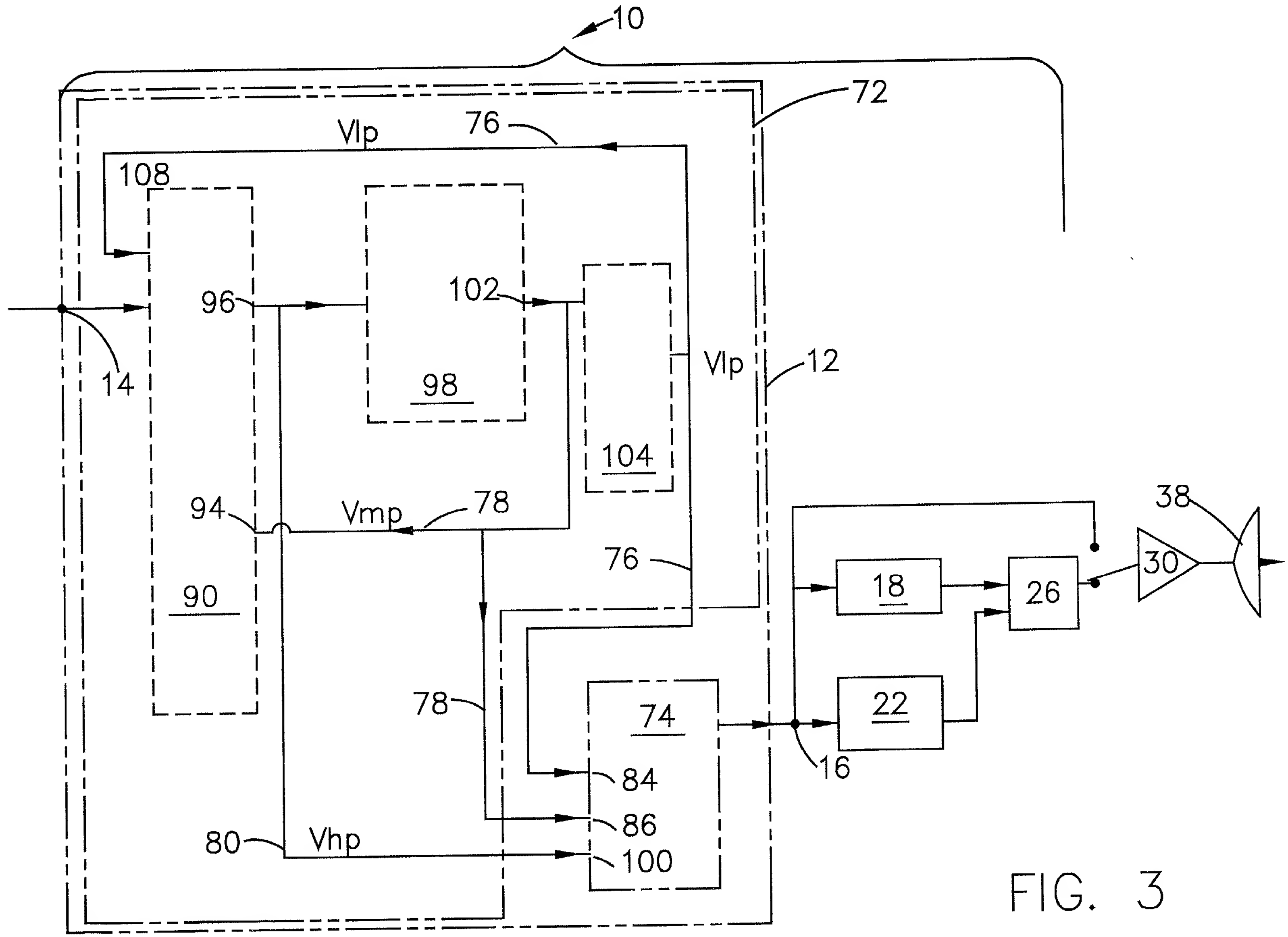
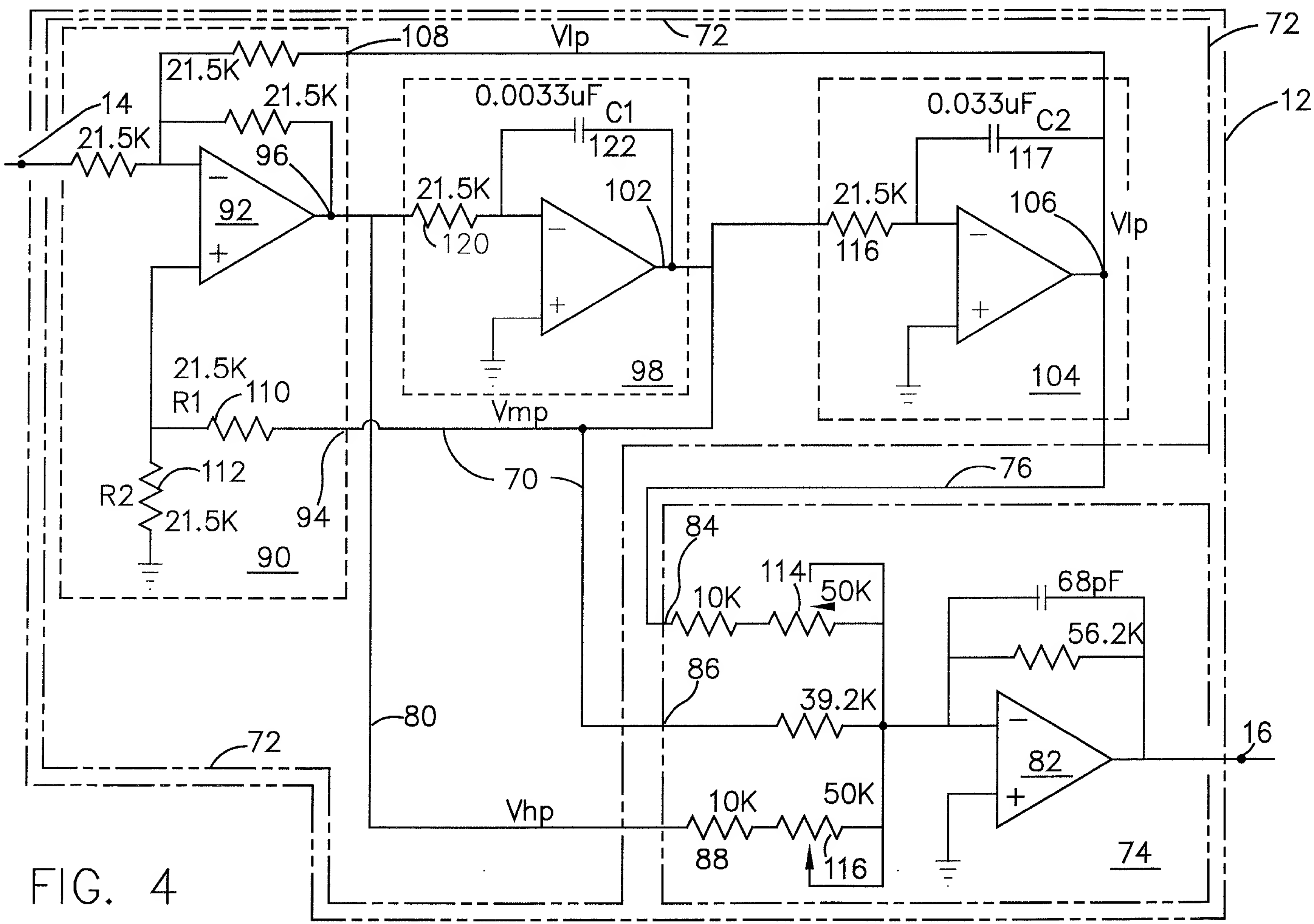


10
72
Vlp
76
108
96
102
98
104
14
Vlp
12
94
Vmp
78
38
76
90
18
26
30
74
22
78
84
16
86
80
Vhp
100

FIG. 3



108
Vlp
72
72
12
14
21.5K
21.5K
21.5K
96
92
0.0033uF
C1
122
21.5K
120
102
98
0.033uF
C2
117
21.5K
116
106
Vlp
104
21.5K
R1
110
Vmp
R2
112
21.5K
94
90
70
76
84
114
10K
50K
68pF
56.2K
86
39.2K
82
16
80
72
Vhp
10K
50K
88
116
74

FIG. 4

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DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

AN AUDIO BOOST CIRCUIT

the specification of which is attached hereto unless the following box is checked:

was filed on ________ as United States Application Number or PCT International Application Number ____________ and was amended on ____________ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is known by me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

NUMBER	COUNTRY	DAY/MONTH/YEAR FILED	PRIORITY CLAIMED

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

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Attorney Docket No.

APPLICATION NO.	FILING DATE

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is known by me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

APPLICATION SERIAL NO.	FILING DATE	STATUS: PATENTED, PENDING, ABANDONED
09/439,119	11/12/99	PENDING

I hereby appoint as my attorneys, with full powers of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Stephen A. Bent, Reg. No. 29,768; David A. Blumenthal, Reg. No. 26,257; William T. Ellis, Reg. No. 26,874; John J. Feldhaus, Reg. No. 28,822; Patricia D. Granados, Reg. No. 33,683; John P. Isacson, Reg. No. 33,715; Eugene M. Lee, Reg. No. 32,039; Richard Linn, Reg. No.25,144; Peter G. Mack, Reg. No. 26,001; Brian J. McNamara, Reg. No. 32,789; Sybil Meloy, Reg. No. 22,749; George E. Quillin, Reg. No. 32,792; Colin G. Sandercock, Reg. No. 31,298; Bernhard D. Saxe, Reg. No. 28,665; Charles F. Schill, Reg. No. 27,590; Richard L. Schwaab, Reg. No. 25,479; Arthur Schwartz, Reg. No. 22,115; Harold C. Wegner, Reg. No. 25,258.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United

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Attorney Docket No.

States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Post Office Address		

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Post Office Address		

Full Name of Fourth Inventor	Signature of Fourth Inventor	Date
Residence Address		Country of Citizenship
Post Office Address		

Full Name of Fifth Inventor	Signature of Fifth Inventor	Date
Residence Address		Country of Citizenship
Post Office Address		

Certificate Under 37 CFR 3.73(b)

Applicant: Paul R. Gagon

Application No.: ______ Filed: ______

For: AN AUDIO BOOST CIRCUIT

BBE SOUND, INC , a California Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of either:

A. [X] An assignment from the inventor(s) of the patent application identified above. The assignment was recorded in the Patent and Trademark Office at Reel ______ , Frame ______, or for which a copy thereof is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application identified above, to the current assignee as shown below:

1. From: ______ To: ______
   The document was recorded in the Patent and Trademark Office at Reel ______ , Frame ______ , or for which a copy thereof is attached.

2. From: ______ To: ______
   The document was recorded in the Patent and Trademark Office at Reel ______ , Frame ______ , or for which a copy thereof is attached.

3. From: ______ To: ______
   The document was recorded in the Patent and Trademark Office at Reel ______ , Frame ______ , or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[ ] Copies of assignments or other documents in the chain of title are attached.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) is empowered to sign this certificate on behalf of the assignee.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: November 12, 1999

Name: John C. McLaren

Title: Chairman/CEO

Signature: ______